

(2)

(11) Publication Number of Patent Application:

JP-A-2001-282206

(43) Date of Publication of Application: October 12, 2001

(54) [Title of the Invention]

LIQUID CRYSTAL DISPLAY DEVICE AND DRIVING CIRCUIT THEREOF

(57) [Abstract]

[Task] To reduce power consumption by preventing unnecessary charge and discharge currents from flowing.

[Means for Resolution] A counter electrode opposed to pixel electrodes is divided into the number equal to the number of gate bus lines 4 and is disposed in parallel with the gate bus lines, the counter electrode portions C1, C2, ..., and Cn are insulated from each other, and a predetermined voltage is applied to each of the counter electrode portions. An ON voltage is applied only to the counter electrode portions corresponding to the ON-state gate bus line 4. When the gate bus line is in an OFF state, the corresponding counter electrode portion is turned to a high impedance state.

[Claims]

[Claim 1]

A liquid crystal display device comprising a pair of substrates opposed to each other and a liquid crystal layer interposed therebetween, in which one substrate is provided with a plurality of gate bus lines and a plurality of source bus lines to intersect with each other with an insulating film interposed therebetween, and switching elements electrically connected to the gate bus lines and the source bus lines and pixel electrodes electrically connected to the switching elements are provided in matrix-form regions divided by the gate bus lines and the source bus lines, respectively, and the other substrate is provided with a counter electrode opposed to the pixel electrodes, the counter electrode is divided into the number equal to the number of gate bus lines and are disposed in parallel with the gate bus lines, the counter electrode portions are insulated from each other, and a predetermined voltage is applied to each of the counter electrode portions,

wherein when an ON voltage is applied to any n-th gate bus line to turn the switching elements electrically connected to the gate bus line to an ON state, an ON voltage for turning the counter electrode portion to an ON state is applied only to the counter electrode portion corresponding to the n-th gate bus line; and

wherein when an OFF voltage is applied to the n-th gate

bus line to turn the switching elements electrically connected to the gate bus line to an OFF state and an ON voltage is applied to the next  $(n+1)$ -th gate bus line and the subsequent gate bus lines to turn the switching elements electrically connected to the gate bus line to an ON state, the counter electrode portion corresponding to the  $n$ -th gate bus line is turned to a high impedance state.

[Claim 2]

The liquid crystal display device according to Claim 1, wherein the pixel electrodes connected through the switching elements electrically connected to the  $n$ -th gate bus line and the  $(n+1)$ -th gate bus line are driven by a line inversion for each of the gate bus lines adjacent to each other by inverting polarities of driving voltages, and voltages having opposite polarities are applied to the  $n$ -th counter electrode and the  $(n+1)$ -th counter electrode to be inverted for each frame.

[Claim 3]

The liquid crystal display device according to Claim 1 or 2, wherein a DC signal is applied as the OFF signal of the gate bus line.

[Claim 4]

The liquid crystal display device according to any one of Claims 1 to 3, further comprising one counter electrode driving circuit, wherein an ON voltage is supplied only to a predetermined counter electrode portion by switching the

counter electrode driving circuit.

[Claim 5]

The liquid crystal display device according to Claim 4, wherein the counter electrode driving circuit also serves as a gate electrode driving circuit for supplying a voltage to the gate bus lines.

[Claim 6]

A driving circuit used for the liquid crystal display device according to any one of Claims 1 to 5, wherein the driving circuit drives the counter electrode and supplies an ON voltage only to a predetermined counter electrode portion by switching.

[Claim 7]

The driving circuit according to Claim 6, wherein the driving circuit also supplies a voltage to the gate bus lines.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Belongs]

The present invention relates to a liquid crystal display device used as a display device for OA (Office Automation) or AV (Audio Visual) and a driving circuit thereof, and particularly, to a so-called active-matrix type liquid display device and a driving circuit thereof, in which switching elements are disposed in a matrix form on a transparent insulating substrate.

[0002]

[Prior Art]



Recently, liquid crystal display devices have been widely used because of characteristics of a thin size, a light weight, and low power consumption. An active-matrix type liquid crystal display device having a switching element disposed for each pixel in a matrix form can provide a high-quality picture in addition to the characteristics, which has attracted attention as the display device used for OA or AV.

[0003]

The general active-matrix type liquid crystal display device is provided with a liquid crystal panel with a liquid crystal layer interposed between two substrates made of insulating materials having translucency such as glass. The back side of the liquid crystal panel is provided with light illuminating means including a light source and a light guide plate in which light emitted from the light source evenly reaches the whole liquid crystal layer and the intensity of light is controlled to be regular, so that the light is uniformly radiated to at least the liquid crystal layer.

[0004]

On one substrate of the liquid crystal panel, a plurality of gate bus lines and a plurality of source bus lines are wired in a matrix form at high density so as to intersect with each other (generally, perpendicular to each other) and are insulated from each other. In the vicinity of the intersecting portion of the bus lines, TFT (thin film transistor) elements serving

as switching elements and pixel electrodes are provided in the matrix divided by the bus lines. The TFT elements are electrically connected to the gate bus lines, the source bus lines, and the pixel electrodes, respectively.

[0005]

On the other substrate, a counter electrode opposed to the pixel electrodes is disposed with a solid pattern on the whole substrate. Peripheral portions of the two substrates are adhered to each other with a sealing agent, and the liquid crystal layer is interposed therebetween.

[0006]

Hereinafter, a process for obtaining a displayed picture using the liquid crystal display device will be described with reference to Figs 3, 4, and 5. Herein, a case of black display will be described.

[0007]

A control circuit 1 shown in Fig. 3 receives arbitrary display data outputted from a signal generating device such as a personal computer and a synchronization signal outputted in a form synchronized with the display data, and the control circuit 1 converts the signal therein into a signal suitable for the liquid crystal display device. Then, predetermined signals are supplied to a gate electrode driving circuit 10, a source electrode driving circuit 2, and a counter electrode driving circuit 11 in the next stage, respectively.

[0008]

The gate electrode driving circuit 10 sequentially applies voltages to gate bus lines ( $G_1, G_2, \dots, G_n$ ) 4. Seeing variation in liquid-crystal voltage 22 applied to a specific pixel with reference to Figs. 4 and 5, an ON voltage represented by a gate signal 20 is applied to a gate electrode G of a TFT element 7 connected to the gate bus line 4 and thus the TFT element 7 is turned to an ON state.

[0009]

At this time, a source signal 14 is applied from the source electrode driving circuit 2 through each source bus line ( $S_1, S_2, \dots, S_m$ ) 6 and the TFT element 7 to a liquid crystal capacitor 8 and an auxiliary capacitor 9 for each pixel, which are a liquid crystal layer portion interposed between the pixel electrode and the counter electrode. A common counter electrode signal (VCOM) 21 is supplied from the counter electrode driving circuit 11 through a counter electrode bus line 5 to the liquid crystal capacitor 8 and the auxiliary capacitor 9. Accordingly, potential differences 16 and 17 as the liquid-crystal applied voltage 22 between the source signal 14 and the counter electrode signal 21 are generated between a predetermined pixel electrode and the counter electrode. In the liquid-crystal applied voltage 22, arrows 16 and 17 represent directions of electric potential, a solid line represents pixel electrode potential (drain waveform) 18a, and a broken line represents a counter

electrode waveform.

[0010]

The potential differences 16 and 17 generated between the source signal 14 and the counter electrode signal (VCOM) 21 are regular, but the signals invert (16, 17) the direction (polarity) of the applied potential 22 for each one field and invert the direction of the potential 22 applied from portions adjacent to each other of the gate bus line 4 for each one line. The reason is to suppress that characteristics deteriorate when a constant DC voltage is applied to a liquid crystal for a long time, and that voltage of the pixel fluctuates due to charge and discharge currents of parasitic capacitors resulting in flicker or the like.

[0011]

On the basis of the counter electrode signal 21 inverted for each one line, the electric potential of the liquid-crystal applied voltage 22 shown in Fig. 4 is changed according to the counter electrode signal 21 by while keeping the potential differences 17 and 16. Accordingly, in order to cancel charge movement of a parasitic capacitor 24 having a large influence according to the TFT element 7 shown in Fig. 5, an OFF signal of the gate signal 20 shown in Fig. 4 also drives an alternating operation with the potential difference of the counter electrode signal 21.

[0012]

The auxiliary capacitor 9 is provided to relieve the fluctuation of the liquid-crystal applied voltage due to fluctuation of parasitic capacitors 23, 24, and 25 as shown in Fig. 5 since the amount of charges kept in the liquid crystal capacitor 8 is small. Although not particularly described in the present specification, an auxiliary capacitor has capacitance between the gate bus line and the pixel electrodes.

[0013]

According to such a driving manner, the light radiated onto the upper surface of the liquid crystal panel is made incident to the liquid crystal through a polarizing plate attached to the liquid crystal panel. An alignment state of liquid crystal molecules is changed with the potential difference generated between each pixel electrode and the counter electrode (VCOM) and the light, a polarizing direction of which is properly changed, is emitted through the other polarizing plate attached to the liquid crystal panel. As a result, it is possible to specific transmission light.

[0014]

[Problem that the Invention is to Solve]

In the aforementioned prior liquid crystal display device, the polarities of the common voltage (counter electrode signal (VCOM)) and the data signal voltage (source signal) are frequently inverted to drive the alternating operation. For this reason, when the voltages are inverted, electric power

is consumed since the charge and discharges currents flow in the liquid crystal panel serving as a capacitive load.

[0015]

Recently, a frequency for inverting the polarities of the common voltage and the data signal voltage has become higher according to high precision. However, since the charge and discharge currents increase in proportion to the frequency, it is difficult to disregard increase in power consumption according to increase in charge and discharge currents.

[0016]

In order to improve the power consumption, for example, JP-A-6-149174 discloses a method of dividing a counter electrode into a plurality of groups and applying voltages so that polarities of the voltages applied to the groups are opposite to each other. In the present line, a line inversion is performed so that the polarities of the driving voltage of the data line (source line) are opposite to each other in  $m$  line and  $m+1$  line, and each inverse polarity is inverted for each frame in two counter electrodes (common electrodes). According to the aforementioned method, since it is possible to drive all the counter electrodes having the same polarity on every other line. Even when the polarities of the counter electrodes are only changed for each one frame, it is possible to drive a low-frequency operation and thus it is possible to reduce power consumption.

[0017]

However, in the aforementioned prior method, it is necessary to constantly apply a voltage to the counter electrode even after a predetermined voltage is applied to a specific liquid crystal capacitor 8 and an auxiliary capacitor 9. Therefore, it is difficult to reduce power consumption of the counter electrode driving circuit itself as much as the applied voltage. In addition, it is difficult to reduce power consumption due to leak currents (the aforementioned charge and discharge currents) in the liquid crystal panel. Further, only one circuit has been necessary so far, but two or more circuits are necessary since the counter electrode is divided. Consequently, there is increase in cost, or increase in area occupied by circuits in a circuit board.

[0018]

The invention has been made to solve the aforementioned problems, and an object of the invention is to provide a liquid crystal display device and a driving circuit thereof, in which it is possible to reduce power consumption by preventing unnecessary charge and discharge currents from flowing, it is possible to reduce power consumption of a counter electrode driving circuit itself, and it is possible to reduce cost and area occupied by circuits in a circuit board.

[0019]

[Means for solving the Problem]

According to the invention, there is provided a liquid crystal display device including a pair of substrates opposed to each other and a liquid crystal layer interposed therebetween, in which one substrate is provided with a plurality of gate bus lines and a plurality of source bus lines to intersect with each other with an insulating film interposed therebetween, and switching elements electrically connected to the gate bus lines and the source bus lines and pixel electrodes electrically connected to the switching elements are provided in matrix-form regions divided by the gate bus lines and the source bus lines, respectively, and the other substrate is provided with a counter electrode opposed to the pixel electrodes, the counter electrode is divided into the number equal to the number of gate bus lines and are disposed in parallel with the gate bus lines, the counter electrode portions are insulated from each other, and a predetermined voltage is applied to each of the counter electrode portions, wherein when an ON voltage is applied to any n-th gate bus line to turn the switching elements electrically connected to the gate bus line to an ON state, an ON voltage for turning the counter electrode portion to an ON state is applied only to the counter electrode portion corresponding to the n-th gate bus line; and wherein when an OFF voltage is applied to the n-th gate bus line to turn the switching elements electrically connected to the gate bus line to an OFF state and an ON voltage is applied to the next (n+1)-th gate bus line

and the subsequent gate bus lines to turn the switching elements electrically connected to the gate bus line to an ON state, the counter electrode portion corresponding to the n-th gate bus line is turned to a high impedance state.

[0020]

In the liquid crystal display device, the pixel electrodes connected through the switching elements electrically connected to the n-th gate bus line and the (n+1)-th gate bus line may be driven by a line inversion for each of the gate bus lines adjacent to each other by inverting polarities of driving voltages, and voltages having opposite polarities may be applied to the n-th counter electrode and the (n+1)-th counter electrode to be inverted for each frame.

[0021]

In the liquid crystal display device, the gate bus lines and the counter electrode portions adjacent to each other may have the inverse polarities of the ON voltages, and the polarities of the ON voltages applied to the counter electrodes may be inverted for each frame.

[0022]

In the liquid crystal display device, a DC signal may be applied as the OFF signal of the gate bus line.

[0023]

The liquid crystal display device may further include one counter electrode driving circuit, in which an ON voltage

is supplied only to a predetermined counter electrode portion by switching the counter electrode driving circuit.

[0024]

In the liquid crystal display device, the counter electrode driving circuit may also serve as a gate electrode driving circuit for supplying a voltage to the gate bus lines.

[0025]

According to the invention, there is provided a driving circuit used for the liquid crystal display device, in which the driving circuit drives the counter electrode and supplies an ON voltage only to a predetermined counter electrode portion by switching.

[0026]

In the driving circuit, the driving circuit may also supply a voltage to the gate bus lines.

[0027]

Hereinafter, an operation of the invention will be described.

[0028]

In an embodiment to be described later of the invention, as shown in Fig. 1, a counter electrode opposed to pixel electrodes is divided into the number equal to the number of gate bus lines 4 and disposed in parallel with the gate bus lines 4. The counter electrode portions are insulated from each other, and a predetermined voltage is applied to each of

the counter electrode portions.

[0029]

In the liquid crystal display device, when an ON voltage is applied to any n-th gate bus line 4 and switching elements (TFT elements 7) electrically connected to the gate bus line 4 is turned to an ON state, an ON voltage for turning the counter electrode portions to an ON state is applied only to the counter electrode portion corresponding to the n-th gate bus line 4. When an OFF voltage is applied to the n-th gate bus line 4 to turn the TFT elements 7 electrically connected to the gate bus line 4 to an OFF state and an ON voltage is applied to the next (n+1)-th gate bus line 4 and the subsequent gate bus lines to turn the switching elements electrically connected to the gate bus line 4 to an ON state, the counter electrode portion corresponding to the n-th gate bus line 4 is turned to an OFF state (high impedance state) 19.

[0030]

Accordingly, after a predetermined voltage is applied to any pixel, the pixel is turned to an OPEN state. Therefore, since unnecessary charge and discharge currents are removed, it is possible to reduce power consumption.

[0031]

Since the ON voltage may be applied only to the counter electrode portion corresponding to the ON-state gate bus line 4, it is possible to largely reduce power consumption of the

counter electrode driving circuit itself. While the OFF voltage is applied to the gate bus line 4, there is no influence of the parasitic capacitor 24 shown in Fig. 5. Accordingly, a DC voltage can be applied as the OFF voltage of the gate bus line. In addition, it is possible to reduce power consumption due to leak currents in the liquid crystal panel.

[0032]

Even when the counter electrode is divided, the ON voltage may be applied only to the counter electrode portion corresponding to the ON-state gate bus line 4. Since the counter electrode driving circuit (common electrode driving circuit) with a small current is switched, it is possible to realize the liquid crystal display device using one circuit. Therefore, it is possible to reduce a cost and an area occupied by circuit in a circuit board.

[0033]

In any n-th gate bus line and the (n+1)-th gate bus line, the pixel electrodes connected through the switching elements electrically connected to the gate bus line are driven by a line inversion for each of the gate bus lines adjacent to each other with driving voltages having opposite polarities, and a predetermined potential is applied to the liquid crystal the n-th gate bus line. Then, when the next (n+1)-th gate bus line and the subsequent gate bus lines are turned to an ON state, the n-th counter electrode portion corresponding to the n-th

gate bus line is turned to an OFF state (high impedance state) and the voltages applied to the liquid crystal is kept. Accordingly, since there is no influence of the parasitic capacitor generated between the pixel electrode and the gate bus line, it is possible to use a DC voltage as the OFF signal of the gate bus line. Therefore, even when the polarity of the signal of each of the counter electrode portions is only changed for each one frame, it is possible to perform a low-frequency drive, thereby reducing power consumption.

[0034]

In an embodiment to be described later, as shown in Fig. 1, the gate electrode driving circuit and the counter electrode driving circuit can be integrated into one circuit. Therefore, it is possible to further reduce an area occupied by the circuit in a circuit board.

[0035]

[Mode for Carrying Out the Invention]

Hereinafter, an embodiment of the invention will be described by way of example, but the invention is not limited to the following example.

[0036]

A liquid crystal display device of the invention includes a liquid crystal panel with a liquid crystal layer interposed between two substrates made of insulating materials with transparency such as glass, as a schematic configuration. The

back side of the liquid crystal panel is provided with light illuminating means including a light source and a light guide plate in which light emitted from the light source evenly reaches the whole liquid crystal layer and the intensity of light is controlled to be regular, so that the light is uniformly radiated to at least the liquid crystal layer.

[0037]

On one substrate of the liquid panel, a plurality of gate bus lines and a plurality of source bus lines are wired in a matrix form at high density so as to intersect with each other (herein, perpendicular to each other) and are insulated from each other. In the vicinity of the intersecting portion of the bus lines, TFT (thin film transistor) elements serving as switching elements and pixel electrodes are provided in the matrix divided by the bus lines. The TFT elements are electrically connected to the gate bus lines, the source bus lines, and the pixel electrodes, respectively.

[0038]

On the other substrate, a counter electrode opposed to the pixel electrodes is divided into the number equal to the number of gate bus lines and disposed in parallel with the gate bus lines. The counter electrode portions are insulated from each other. For example, a predetermined voltage such as 3-State-Buffer is applied each of the counter electrode portions. Peripheral portions of the two substrates are adhered to each

other with a sealing agent, and a liquid crystal layer is interposed therebetween.

[0039]

A process for obtaining a display picture using the liquid crystal display device will be described with reference to Figs. 1, 2, and 5. In the following figures, the same reference numerals are given to parts having the same function as the prior art shown in Figs. 3 and 4.

[0040]

A control circuit 1 shown in Fig. 1 receives arbitrary display data outputted from a signal generating device such as a personal computer and a synchronization signal outputted in a form synchronized with the display data, and the control circuit 1 converts the signal therein into a signal suitable for the liquid display device. Then, predetermined signals are supplied to a gate/counter electrode driving circuit 3, a source electrode driving circuit 2, and a counter electrode driving circuit 11 in the next stage, respectively.

[0041]

The gate/counter electrode driving circuit 3 sequentially applies voltages to gate bus lines ( $G_1, G_2, \dots, G_n$ ) 4. Seeing variation in liquid-crystal voltage 15 applied to a specific pixel with reference to Figs. 2 and 5, an ON voltage represented by a gate signal 12 shown in Fig. 2 is applied to a gate electrode G of a TFT element 7 connected to the gate bus line 4 and thus

the TFT element 7 is turned to an ON state.

[0042]

At this time, a source signal 14 is applied from the source electrode driving circuit 2 through each source bus line (S<sub>1</sub>, S<sub>2</sub>, ..., S<sub>m</sub>) 6 and the TFT element 7 to a liquid crystal capacitor 8 and an auxiliary capacitor 9 for each pixel, which are a liquid crystal layer portion interposed between the pixel electrode and the counter electrode portions (C<sub>1</sub>, C<sub>2</sub>, ..., C<sub>n</sub>). A counter electrode signal 13 is supplied from the gate/counter electrode driving circuit 3 through a counter electrode bus line 5 to the liquid crystal capacitor 8 and the auxiliary capacitor 9. Accordingly, potential differences 16 and 17 as the liquid-crystal applied voltage 15 between the source signal 14 and the counter electrode signal 13 are generated between a predetermined pixel electrode and the counter electrode portions. In the liquid-crystal applied voltage 15, arrows 16 and 17 represent directions of electric potential, a solid line represents pixel electrode potential (drain waveform) 18, and a broken line represents a counter electrode waveform.

[0043]

The light radiated onto the upper surface of the liquid crystal panel is made incident to the liquid crystal through a polarizing plate attached to the liquid crystal panel. An alignment state of liquid crystal molecules is changed with the potential difference generated between each pixel electrode

and the counter electrode portion and the light, a polarizing direction of which is properly changed, is emitted through the other polarizing plate attached to the liquid crystal panel. As a result, it is possible to specific transmission light.

[0044]

In this case, the potential differences 16 and 17 generated between the source signal 14 and the counter electrode signal 13 are regular, but the signals invert (16, 17) the direction (polarity) of the applied potential 22 for each one field and invert the direction of the potential 22 applied from portions adjacent to each other of the gate bus line 4 for each one line. The reason is to suppress that characteristics deteriorate when a constant DC voltage is applied to a liquid crystal for a long time, and that voltage of the pixel fluctuates due to charge and discharge currents of parasitic capacitors resulting in flicker or the like.

[0045]

When the gate signal 12 of the gate bus line 4 is turned to an ON voltage, the counter electrode signal 13 inverted for each one line is turned to an ON voltage for turning the corresponding counter electrode portion to an ON state. When an ON voltage 19a is applied to the next gate bus line 4 and the gate signal 12 of the gate bus line 4 is turned to an OFF voltage, the corresponding counter electrode portion is turned to an OFF state (high impedance state) 19. For this reason,

as the liquid-crystal applied voltage 22 of the prior example shown in Fig. 4, potential does not fluctuate according to the counter electrode signal 21 while keeping the potential difference 17 or 16. Accordingly, since there is no effect of the parasitic capacitor 24 due to the TFT element 7 shown in Fig. 5, a DC voltage can be used as the OFF signal of the gate signal 12. Therefore, even when the polarities of the counter electrode portions are only changed for each one frame, it is possible to drive a low-frequency operation, and thus it is possible to reduce power consumption.

[0046]

After a predetermined voltage is applied to a specific liquid crystal capacitor 8 and auxiliary capacitor 9, it is unnecessary that the counter electrode is turned to high impedance and a voltage is applied thereto. Accordingly, it is possible to reduce power consumption of the electrode driving circuit itself as much as the voltage. Therefore, it is possible to suppressed charge and discharge currents of the liquid crystal panel serving as capacitive load and thus it is possible to reduce power consumption. In addition, even when the counter electrode is divided, it is possible to supply an ON voltage only to a predetermined counter electrode portion by switching the one gate/counter electrode driving circuit. Therefore, it is possible to reduce a cost and an area occupied by a circuit in a circuit board.

[0047]

Fig. 6 shows a configuration example of the gate/counter electrode driving circuit 3. In the example, a gate bus line (G1) is active, and the other gate bus lines are non-active.

[0048]

In the circuit, reference sign SW1 denotes a switch for selecting any one signal of a VGH (ON voltage of gate signal) and a VGL (OFF voltage of gate signal), reference sign SW2 denotes a switch for selecting COM (ON voltage of counter electrode signal) or a non-connection state (high impedance state). A delay circuit 31 delays a timing for selecting whether the counter electrode signals C1, C2, ... is made active (ON voltage) or made to be high impedance state, from a variation point of the gate signals G1, G2, .... At this time, the amount of delay substantially corresponds to a delay time of the gate signal in the liquid crystal panel. The delay circuit is provided to prevent the counter electrode signal C1 or the like from being in the high impedance state before the gate signal G1 or the like is completely turned to the OFF voltage.

[0049]

The SW1 and SW2 are switched on the basis of the signals received from the control circuit 1. For example, when the gate bus line G1 and the counter electrode bus line C1 are active (ON), a VGH (ON voltage of gate signal) and a COH (counter electrode signal) are outputted to the lines G1 and C1,

respectively. In order to output the signal at the optimum timing, the signal is outputted through the delay circuit 31 to the counter electrode bus line C1. At this time, a VGL (OFF voltage of gate signal) and an OPEN (high impedance) are outputted to the other gate bus lines G2, G3, ... and the other counter electrode bus lines C2, C3, ..., respectively.

[0050]

Accordingly, as output states of the COH (counter electrode signal), three levels are outputted such as the two level ON states (Hi level/ Lo level) and the OFF state (high impedance).

[0051]

With such a circuit configuration, since it is possible to scan all the gate signals and the counter electrode signals using the same (single) shift registers, it is not necessary to provide additional shift registers to scan the counter electrode signals. In addition, it is possible to perform an accurate timing synchronization between the gate signals and the counter electrode signals.

[0052]

In the aforementioned embodiment, the case of black display is described, but the invention is applicable to a case of white display or gradation display. The auxiliary capacitor 9 has capacitance between the counter electrode and the pixel electrodes, but the auxiliary capacitor 9 may have capacitance

between the gate bus line and the pixel electrodes.

[0053]

[Advantage of the Invention]

As described above in detail, according to the invention, there is provided the liquid crystal display device including a counter electrode opposed to the pixel electrodes, in which the counter electrode is divided into the number equal to the number of gate bus lines and are disposed in parallel with the gate bus lines, the counter electrode portions are insulated from each other, and a predetermined voltage is applied to each of the counter electrode portions, wherein an ON voltage is applied only to the counter electrode portion corresponding to the ON-state gate bus line, and the corresponding counter electrode portion is turned to an OFF state (high impedance) when the gate bus line is in an OFF state, thereby keeping an liquid-crystal applied voltage. Therefore, since unnecessary charge and discharge currents are removed, it is possible to largely reduce power consumption.

[0054]

The ON voltage may be applied only to the counter electrode portion corresponding to the ON-state gate bus line. Accordingly, while the OFF voltage is applied to the gate bus line, there is no influence of the parasitic capacitor. Therefore, it is possible to use a DC voltage as the OFF signal of the gate bus line. Consequently, it is possible to largely

reduce power consumption of the counter electrode driving circuit itself. In addition, it is possible to reduce power consumption due to a leak current or the like in the liquid crystal panel.

[0055]

Further, even when the counter electrode is divided, the ON voltage may be applied only to the counter electrode portion corresponding to the ON-state gate bus line. Since the counter electrode driving circuit with a small current is switched, it is possible to realize the liquid crystal display device using one circuit. Therefore, it is possible to reduce a cost and an area occupied by a circuit in a circuit board.

[Brief Description of the Drawings]

[Fig. 1] Fig. 1 is a block diagram illustrating an inner circuit configuration of a liquid crystal panel and a circuit configuration in the vicinity thereof, in a liquid crystal display device according to an embodiment of the invention.

[Fig. 2] Fig. 2 is a timing chart illustrating operations for signals in a specific pixel, in a liquid crystal display device according to an embodiment of the invention.

[Fig. 3] Fig. 3 is a block diagram illustrating an inner circuit configuration of a liquid crystal panel and a circuit configuration in the vicinity thereof, in the prior liquid crystal display device.

[Fig. 4] Fig. 4 is a timing chart illustrating operations

for signals in a specific pixel, in the prior liquid crystal display device.

[Fig. 5] Fig. 5 is a block diagram illustrating a transmission circuit in the vicinity of a TFT element.

[Fig. 6] Fig. 6 is a block diagram illustrating an example of an inner configuration of a gate/counter electrode driving circuit 3, in a liquid crystal display device according an embodiment of the invention.

[Description of Reference Numerals and Signs]

1: CONTROL CIRCUIT

2: SOURCE ELECTRODE DRIVING CIRCUIT

3: GATE/COUNTER ELECTRODE DRIVING CIRCUIT

4: GATE BUS LINE

5: COUNTER ELECTRODE BUS LINE

6: SOURCE BUS LINE

7: TFT ELEMENT

8: LIQUID CRYSTAL CAPACITOR

9: AUXILIARY CAPACITOR

10: GATE ELECTRODE DRIVING CIRCUIT

11: COUNTER ELECTRODE DRIVING CIRCUIT

12, 20: TIMING CHART OF GATE SIGNAL

13, 21: TIMING CHART OF COUNTER ELECTRODE SIGNAL

15, 22: LIQUID CRYSTAL APPLYING VOLTAGE

16: LIQUID CRYSTAL APPLYING VOLTAGE HAVING POLARITY INVERSE

TO 17

17: LIQUID CRYSTAL APPLYING VOLTAGE HAVING POLARITY INVERSE  
TO 16

18, 18a: TIMING CHART OF PIXEL ELECTRODE POTENTIAL

19: OFF STATE (HIGH IMPEDANCE STATE) OF COUNTER ELECTRODE

23: PARASITIC CAPACITOR BETWEEN GATE AND SOURCE

24: PARASITIC CAPACITOR BETWEEN GATE AND DRAIN

25: PARASITIC CAPACITOR BETWEEN SOURCE AND DRAIN

31: DELAY CIRCUIT

G1: GATE BUS LINE OF FIRST LINE

G2: GATE BUS LINE OF SECOND LINE

Gn: GATE BUS LINE OF n-th LINE

S1: SOURCE BUS LINE OF FIRST LINE

S2: SOURCE BUS LINE OF SECOND LINE

Sm: SOURCE BUS LINE OF m-th LINE

VCOM: COMMON COUNTER ELECTRODE

C1: COUNTER ELECTRODE BUS LINE OF FIRST LINE

C2: COUNTER ELECTRODE BUS LINE OF SECOND LINE

Cn: COUNTER ELECTRODE BUS LINE OF n-th LINE

G: GATE OF TFT ELEMENT

S: SOURCE OF TFT ELEMENT

D: DRAIN OF TFT ELEMENT

SW1, SW2: SWITCH